UART-AXI4-Stream IP — Debug & Fix Specification

# 1. Introduction

This document instructs a junior RTL engineer to identify, fix, and verify ten intentionally injected functional bugs in a UART-AXI4-Stream IP block. The IP includes a transmitter (TX), receiver (RX), and a lightweight top integrating both over a shared prescaler. The target is to deliver a robust, parameterized UART operating with LSB-first framing, mid-bit sampling, and standards-compliant AXI4-Stream handshakes.

# 2. Scope & Objectives

- Bring the IP to functional correctness for 8-bit frames (default) and validate parameter robustness up to 16 bits.

- Ensure clean CDC for asynchronous RXD and synchronous resets.

- Enforce AXI4-Stream ready/valid semantics on TX and RX interfaces.

- Provide regression tests that catch each bug deterministically.

- Deliver lint-clean RTL conforming to the naming and style in Section 9.

# 3. External Interface:

Common ports used by TX/RX/top:

|  |  |  |
| --- | --- | --- |
| Port | Dir | Description |
| clk | input | System clock. |
| rst | Input | Active-high synchronous reset. |
| prescale[15:0] | Input | Baud prescale unit; bit time = 8\*prescale cycles. |
| s\_axis\_tdata[DATA\_WIDTH-1:0] | Input | TX payload. |
| s\_axis\_tvalid | Input | TX payload valid. |
| s\_axis\_tready | output | TX ready (assert in idle, deassert during shift). |
| txd | Output | UART TX line (idle=1). |
| m\_axis\_tdata[DATA\_WIDTH-1:0] | Output | RX payload. |
| m\_axis\_tvalid | Output | RX payload valid. |
| m\_axis\_tready | Input | RX consumer ready. |
| rxd | Input | UART RX line (idle=1). |
| tx\_busy | Output | TX busy (active during start, data, stop). |
| rx\_busy | Output | RX busy. |
| rx\_overrun\_error | Output | RX overrun flag. |
| rx\_frame\_error | Output | RX framing error flag. |

Note: The prescale convention assumes the RTL loads a counter with (prescale<<3)-1 to generate one bit-time.

# 4. UART Frame & Timing Requirements

- Idle level: 1. Start bit: 0. Data: LSB first. Stop bit: 1 (one stop bit).

- TX must hold each bit for exactly one bit-time; RX must sample mid-bit.

- RX sampling schedule: on start detect, wait 1.5 bit-times for d0, then sample every 1.0 bit-time.

- RX must double-flop synchronize RXD before any FSM logic.

# 5. Bug Inventory (to be fixed)

BUG 1 — Prescaler off-by-one: Bit time loaded with (prescale<<3) instead of ((prescale<<3)-1).

BUG 2 — MSB-first transmit: Shift direction makes MSB leave first; wire order reversed.

BUG 3 — AXI tready toggling: TX toggles tready in idle; violates ready/valid contract.

BUG 4 — Narrow counter: Bit counter too small for DATA\_WIDTH>15; wraps early.

# 6. Fix Plan (per bug)

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| --- | --- | --- | --- |
| Bug | Root Cause | Code-Level Fix | Acceptance Criteria |
| 1 | Reload value for bit-time lacks -1. | Use (prescale<<3)-1 for start/data/stop loads; unify helper function or localparam. | Measured bit period matches expected within ±1 clk; no RX framing at nominal jitter. |
| 2 | Left shift / MSB-first. | Shift right with {1'b0, shreg\_q} and drive tx from shreg\_q[0] style, or rotate as shown in reference. | Loopback of 0x55/0xAA/0x00/0xFF returns identical bytes. |
| 4 | Improper ready toggling. | Hold tready=1 in idle; set 0 only while shifting. | AXI handshake coverpoints: no duplicate or lost frames. |
| 5 | Overrun flag management. | Set overrun when valid\_q=1 and new byte completes; clear when consumer handshakes or on reset. | Overrun asserts only when unread data exists; clears on read. |

# 7. Implementation Guidance

1. Introduce helper functions or localparams for consistent prescale reloads.
2. Use explicit “\*\_q” register naming; avoid mixing comb and seq logic in one always block unless sequential-only.
3. Keep TX “tready” asserted in idle; deassert while “busy\_q==1”.
4. In RX, clear “valid\_q” only on (valid && ready).
5. Status flag policy:

• frame\_error\_q: set when stop==0; clear on next start or reset.

• overrun\_q: set when (valid\_q==1) and new byte completes; clear on read handshake.

# 8. Verification Plan

Testbench: clock 50 MHz, default prescale=54 → 115200 baud. Provide tasks to push/pop AXI, inject bytes on RXD, and loopback TX→RX.

|  |  |  |
| --- | --- | --- |
| Test ID | Purpose | Pass Criteria |
| T1 | Bit-time accuracy (BUG1) | Measured bit period within ±1 cycle; RX no framing. |
| T2 | Bit order (BUG2) | Loopback returns identical bytes for patterns 0x55,0xAA,0x00,0xFF. |
| T3 | RX sampling phase (BUG3) | ±5% baud skew still clean; no bit flips. |
| T4 | AXI handshake (BUG4) | No duplicate/lost packets across random ready/valid backpressure. |
| T5 | Overrun lifecycle (BUG5) | Overrun asserts only when unread data overwritten; clears on read. |
| T6 | CDC stability (BUG6) | Glitch injection on RXD does not disturb sampling due to 2-FF sync. |
| T7 | Parameter width (BUG7) | DATA\_WIDTH=16 passes loopback and waveform shows correct length. |
| T8 | Busy stop behavior (BUG8) | No enqueue accepted until full stop completed; no merged frames. |
| T9 | Start detection (BUG9) | Short low start accepted; noise-spike immunity maintained. |
| T10 | Stop polarity (BUG10) | frame\_error only when stop forced low at end of frame. |

Add assertions:

• TX: tready high only when !busy\_q; busy high from start through end of stop.

• RX: first sample at 1.5T; subsequent samples at 1.0T.

• RX: once valid\_q=1, data stable until (valid&&ready).

# 09. Deliverables

- Fixed RTL for TX, RX, and top with comments summarizing changes.

- Self-checking testbench with tasks and assertions mapped to tests T1–T10.

- Waveform snapshots for at least: start→d0 at 1.5T, LSB-first stream, stop bit high, tready/busy timing.

- Short README: how to run sims, expected console output, and pass/fail criteria.

# 10. Definition of Done (DoD)

• All tests T1–T10 pass in regression across two baud settings (e.g., 115200 and 3M).

• Lint (basic) passes: no unused nets, no latch inference, no CDC warnings on RX path.

• Code reviewed; style and naming follow Section 9.

• Version tagged and changelog updated.